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Terms	Documents
L1 same (message or instruction or command)	32

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<u>L2</u>	L1 same (message or instruction or command)	32	<u>L2</u>
<u>L1</u>	processor same initializ\$3 same controller same disabl\$3	69	<u>L1</u>

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L1 710/305,104,313-
 315,10,110;711/100,147,154;361/683,686;713/1;709/208;719/321,327;712/32,36;370/257,453.ccls. 14840 L1

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Terms	Documents
L1 and L2	7

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<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L3</u> 11 and L2	7	<u>L3</u>
<u>L2</u> processor same initializ\$3 same controller same disabl\$3	69	<u>L2</u>
<u>L1</u> 710/305,104,313- 315,10,110;711/100,147,154;361/683,686;713/1;709/208;719/321,327;712/32,36,370/257,453.ccls.	14840	<u>L1</u>

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Drews, P.; Fromm, P.;

Industrial Electronics, Control and Instrumentation, 1997. IECON 97. 23rd International Conference on Volume 3, 9-14 Nov. 1997 Page(s):1275 - 1277 vol.3

Digital Object Identifier 10.1109/IECON.1997.668494

[AbstractPlus](#) | [Full Text: PDF\(288 KB\)](#) **IEEE CNF****2. A formal approach to MpSoC performance verification**

Richter, K.; Jersak, M.; Ernst, R.;

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Volume 36, Issue 4, April 2003 Page(s):60 - 67

Digital Object Identifier 10.1109/MC.2003.1193230

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(365 KB\)](#) **IEEE JNL****3. Fuzzy logic based position control of permanent magnet synchronous motor**

Uddin, M.N.; Radwan, T.S.; Rahman, M.A.; George, G.H.;

Electrical and Computer Engineering, 2000 Canadian Conference on

Volume 1, 7-10 March 2000 Page(s):93 - 97 vol.1

Digital Object Identifier 10.1109/CCECE.2000.849677

[AbstractPlus](#) | [Full Text: PDF\(420 KB\)](#) **IEEE CNF****4. Architectural and compiler techniques for energy reduction in high-performance microprocessors**

Bellas, N.; Hajj, I.N.; Polychronopoulos, C.D.; Stamoulis, G.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

Volume 8, Issue 3, June 2000 Page(s):317 - 326

Digital Object Identifier 10.1109/92.845897

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(248 KB\)](#) **IEEE JNL****5. A BCI-based environmental controller for the motion-disabled**

Xiaorong Gao; Dingfeng Xu; Ming Cheng; Shangkai Gao;

Neural Systems and Rehabilitation Engineering, IEEE Transactions on [see also IEEE Trans. on Rehabilitation Engineering]

Volume 11, Issue 2, June 2003 Page(s):137 - 140

Digital Object Identifier 10.1109/TNSRE.2003.814449

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(487 KB\)](#) **IEEE JNL****6. Clock controller design in SuperSPARC II microprocessor**

Hao, H.; Bhabuthmal, K.;

Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International Conference on

2-4 Oct. 1995 Page(s):124 - 129

Digital Object Identifier 10.1109/ICCD.1995.528800

[AbstractPlus](#) | Full Text: [PDF\(580 KB\)](#) [IEEE Xplore](#)**7. Rescue: A Microarchitecture for Testability and Defect Tolerance**

Schuchman, E.; Vijaykumar, T.N.;

Computer Architecture, 2005. ISCA '05. Proceedings. 32nd International Symposium on
04-08 June 2005 Page(s):160 - 171

Digital Object Identifier 10.1109/ISCA.2005.44

[AbstractPlus](#) | Full Text: [PDF\(160 KB\)](#) [IEEE Xplore](#)**8. Based digital signal processor to develop the M3S novel kernel system**

Chien-Chi Chen; Jen-Chien Chien; Meng-Lun Hsueh; Jer-Junn Luh; Fok-Ching Chong;

Engineering in Medicine and Biology Society, 2003. Proceedings of the 25th Annual International Conference of the IEEE
Volume 2, 17-21 Sept. 2003 Page(s):1732 - 1733 Vol.2
Digital Object Identifier 10.1109/IEMBS.2003.1279734[AbstractPlus](#) | Full Text: [PDF\(231 KB\)](#) [IEEE Xplore](#)**9. Evolving real-time systems using hierarchical scheduling and concurrency analysis**

Regehr, J.; Reid, A.; Webb, K.; Parker, M.; Lepreau, J.;

Real-Time Systems Symposium, 2003. RTSS 2003. 24th IEEE
2003 Page(s):25 - 36
Digital Object Identifier 10.1109/REAL.2003.1253251[AbstractPlus](#) | Full Text: [PDF\(358 KB\)](#) [IEEE Xplore](#)**10. A low power pseudo-random BIST technique**

Basturkmen, N.Z.; Reddy, S.M.; Pomeranz, I.;

Computer Design: VLSI in Computers and Processors, 2002. Proceedings. 2002 IEEE International Conference on
16-18 Sept. 2002 Page(s):468 - 473
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Chien-Chih Chen Jen-Chien Chen Meng-Lun Hsieh Jen-Jiun Luh Fok-Ching Chong
Inst. of Electr. Eng., Nat. Taiwan Univ., China

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Abstract

The multiple masters multiple slave (M3S) is an intelligent protocol. It provides the disable a concrete integral control for his movement, working, environment control and communication. This is an integrated real time control capability protocol. It is a plug and play device interface. Once plug-in, the new device with integrate and communicate with existing devices in use. Our proposal is aim at this purpose. We intend to design and develop a M3S protocol that meets the requirement lay down in the M3S working group. Integrating different types of tools will absolutely bring lots of comforts to the disable. We set up the system using equipments purchase from the market, tested the system and ready it to be tested by other subgroups.

Index Terms

biomechanics, biomedical communication, biomedical equipment, medical computing, protocols, signal processing

Controlled Indexing

M3S novel kernel system, assistive device, communication, concrete integral control, digital signal processor, environment control, integrated real time control capability protocol, multiple masters, multiple slave protocol

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3	US 6661671 B1	20031209	16	Apparatus, method and article of manufacture	361/752	361/686; 361/796;
4	US 6546483 B1	20030408	8	Method and apparatus for configuring a devic	713/1	710/10
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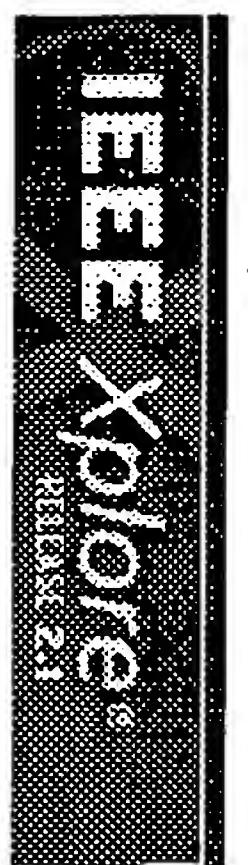
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Author Keywords

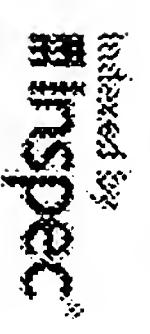
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